REMARKS

Entry of this amendment under the provisions of 37 CFR § 1.114, and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Final Office Action dated January 3, 2003. Following the Final Office Action, a telephone interview was conducted between the Examiner, Mr. Pompey, and Applicants undersigned attorney on April 8, 2003. Appreciation is expressed to Examiner Pompey for his courtesy and helpfulness during this telephone interview. In the course of this interview, the present amendment to claims 42 and 47 was discussed. After reviewing this, Examiner Pompey indicated that this would require further search and/or substantial further consideration on his part. Accordingly, Examiner Pompey indicated that this amendment could not be entered after final rejection. Accordingly, the present Request for Continued Examination (RCE) has been filed.

By the present amendment, claims 42 and 47 have been amended to particularly distinguish over the arrangement taught by the primary reference to Wu, (USP 4,859,619). Accordingly, reconsideration and allowance of independent claims 42 and 47, and their respective dependent claims, is respectfully respected for the reasons set forth below.

Specifically, by the present amendment, each of claims 42 and 47 has been amended to define that the first conductive strip is formed in a separate manufacturing step from the first conductor plugs and the second conductive strip is formed in a separate manufacturing step from the first conductor plugs. This can be appreciated by comparing Figs. 9 and 10 of the present application. For example, in Fig. 9 the first conductor plugs are shown with the numeral 23. As can be appreciated from Fig. 9, these first conductor plugs are filled into the contact holes shown in Fig. 8.

Subsequently, as shown in Fig. 10, the first conductive and the second conductive strip are respectively formed over the first conductor plugs. Thus, as shown in Figs. 9 and 10 and as discussed on pages 14-16 of the specification, the formation of the first and second conductive strips involves a separate manufacturing step from the formation of the first conductor plugs.

In the Office Action, it is indicated on page 2 that all of the conductor plugs, the first conductive strip and the second conductive strip can be read on the metalization layers 81 shown in Fig. 7 of the Wu reference. From Fig. 7 of Wu and the corresponding description it is clear that these metalizations 81 are formed in a single manufacturing step to both fill the contact hole 79 and form conductive portions for subsequent contact arrangements. Thus, it is quite clear that Fig. 7 of Wu cannot read on the amended language that the first conductive strip if formed in a separate manufacturing step from the first conductor plugs and the second conductive strip is formed in a separate manufacturing step from the first conductor plugs.

The significance of this manufacturing difference is clear from the Wu reference. Specifically, as shown in Fig. 7 of Wu, indent regions are created in the metalizations 81 over each of the contact holes. This is a result of the natural flow of the metalization material that leads to an indent in the upper surface of the metalization 81 above each of the contact holes 79. Comparing this with Fig. 10 of the present application, it can be seen that the upper surfaces of the first and second conductive strips (e.g. shown, for example, BL1, BL2, etc.) are smooth without the undesirable indent created in the single piece metalization technique of Wu. Therefore, a distinct structural difference is created in the completed product by the difference in manufacturing steps between the Wu reference and the present invention.

As indicated in the case of *In re Luck*, 177 USPQ 523:

> "As for the method of application, it is well established that product claims may include process steps to wholly or partially define the claim product... to the extent these process limitations distinguish the product over the prior art, they must be given the same consideration as traditional product characteristics." 177 USPQ at 525

In the present instance, the differences in the process of forming the first and second conductive strips in a separate manufacturing step from the first conductor plugs leads to a superior product since the resulting product will not have the undesirable indent shown in the Wu reference. Accordingly, it is respectfully submitted that amended claims 42 and 47 clearly define over Wu.

It also respectfully submitted that nothing in the Ho reference (USP 4,954,214) suggests anything to make up for the above-noted shortcomings of Wu. Ho has been cited for the teaching in column 8, line 35 et. seq. of forming openings "at the predetermined locations where interconnect metal is desired." As particularly noted on page 3 of the Final Office Action:

> "The Examiner takes official notice that forming the second opening over the first conductor plug is a matter of design choice, because photolithographic techniques can form opening anywhere one skilled in the art prefers to put them (see Ho Fig. 4c; column 8, lines 35-45)."

As such, although the teachings of Ho are of general interest regarding the placement of openings, as noted in the Final Office Action, they do not pertain to the above-noted amendments of claims 42 and 47, and would not suggest modification of Wu to arrive at the present claimed invention. With further regard to this, although the Ho references does disclose plugs, the reference is only concerned with CMOS devices, and does not deal with an arrangement, such as defined in both claims 42 and 47, of a first portion for a memory array and a second portion for circuit other than a memory array. So further,

since the respective metalization processes used in Wu and Ho are completely different from one another, one of ordinary skill in the art would not be motivated to modify Wu using Ho due to these differences.

For reasons set forth above, it is respectfully submitted that amended claims 42 and 47, and their dependent claims, clearly define over the combination of Wu and Ho, and reconsideration and allowance of these claims, together with their dependent claims, is respectfully requested.

Attached hereto is a marked-up version of the changes made to the title by the current amendment. The attached page is captioned "Version with markings to show changes made."

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (501.35437CV2).

Respectfully submitted,

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Attachment: Version With Markings To Show Changes Made

ATTACHMENT

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 42 and 47 as follows:

42. (Twice Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions and a gate electrode between said first semiconductor regions;

second semiconductor regions arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said first and second portions;

a plurality of first openings formed simultaneously in said first insulating film above both said first and second portions;

a plurality of first conductor plugs formed in said first openings in said first insulating film on said first semiconductor regions in said first portion and on said second semiconductor regions in said second portion;

a first conductive strip formed on said first insulating film in said first portion and electrically connected to one of the first semiconductor regions of said MISFET through one of said first conductor plugs, wherein said first conductive strip is formed in a separate manufacturing step from said first conductor plugs; and

a second conductive strip formed on said first insulating film in said second portion and electrically connected to said second semiconductor regions through said first conductor plugs to electrically connect said second semiconductor regions to one

another through said second conductive strip, wherein said second conductive strip is formed in a separated manufacturing step from said first conductor plugs;

a second insulating film formed over said first insulating film and said first and second conductive strips;

a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET;

a second conductor plug formed in said second opening in said second insulating film to electrically connect with said one of said first conductor plugs connected to the other of said first semiconductor regions of said MISFET; and

a third conductive strip formed on said second insulating film and electrically connected to said second conductor plug,

wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the second semiconductor regions and the second conductive strip in the second portion.

47. (Twice Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions of n-type conductivity and a gate electrode between said first semiconductor regions;

a second semiconductor region of n-type conductivity and a third semiconductor region of p-type conductivity arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said first and second portions;

a plurality of first openings formed simultaneously in said first insulating film above both said first and second portions;

a plurality of first conductor plugs each comprising a tungsten film formed in said first openings in said first insulating film on said first semiconductor regions in said first portion and on said second semiconductor regions in said second portion;

a first conductive strip formed on said first insulating film in said first portion and electrically connected to one of the first semiconductor regions of said MISFET through one of said first conductor plugs, wherein said first conductive strip is formed in a separate manufacturing step from said first conductor plugs; and

a second conductive strip formed on said first insulating film in said second portion and electrically connected to said second and third semiconductor regions through said first conductor plugs to electrically connect said second and third semiconductor regions to one another through said second conductive strip, wherein said second conductive strip is formed in a separate manufacturing step from said first conductor plugs;

a second insulating film formed over said first insulating film and said first and second conductive strips;

a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET;

a second conductor plug formed in said second opening in said second insulating film to electrically connect with said one of said first conductor plugs connected to the other of said first semiconductor regions of said MISFET; and

a third conductive strip formed on said second insulating film and electrically connected to said second conductor plug,

wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the second semiconductor regions and the second conductive strip in the second portion.